DATA SHEET

PCF7991AT

Advanced Basestation IC (ABIC)

Product Specification

2007 Aug 24

Confidential

CONTENTS

1 FEATURES

- Fully integrated single chip basestation
- Compatible with PCF79xx transponder families (HT2, HT2-Extended, HT-Pro)
- Robust antenna coil power driver stage with modulator
- High performance adaptive sampling time AM/PM demodulator (patent pending)
- Read and write function
- Programmable modulator/demodulator characteristics
- On-chip clock oscillator and divider in the case of external clock reference
- Antenna rupture and short circuit detection
- Low power consumption
- Very low power stand-by mode
- Low external component count
- Small package (SO14)

2 GENERAL DESCRIPTION

The PCF7991AT is a fully integrated Advanced Basestation IC, ABIC, designed for car immobilizer systems providing read and write access to an identification transponder. The device is intended for use with the NXP transponder family (PCF79xx) as well as other transponder types operating at 125 kHz and employing ASK, Amplitude Shift Keying for write and AM/PM for the read operation. The receiver characteristics (amplifier gain, filter cutoff frequencies) can be optimized to system and transponder requirements. The PCF7991AT IC is designed for easy integration into immobilizer read/write and read-only systems featuring a high degree of integration and very low external component count. The device integrates a powerful antenna driver/modulator, a low-noise adaptive sampling time demodulator, programmable filters/amplifier and digitizer, required to design high-performance basestations. A three wire microcontroller interface is provided for programming the PCF7991AT as well as for the bidirectional communication with the transponder. The three-wire interface can be configured for two wire operation by connecting the data input and the data output.

The device employs a unique Adaptive Sampling Time (AST) demodulation technique, that extends the system operation range and eliminates the effect of a zero amplitude modulation response from the transponder, as a result of resonance frequency tolerances.

3 ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			TEMPERATURE RANGE (°C)
	NAME	DESCRIPTION	OUTLINE VERSION	
PCF7991AT/1081	SO14	plastic small outline package; 14 leads	SOT108-1	-40°C to +85°C

4 BLOCK DIAGRAM

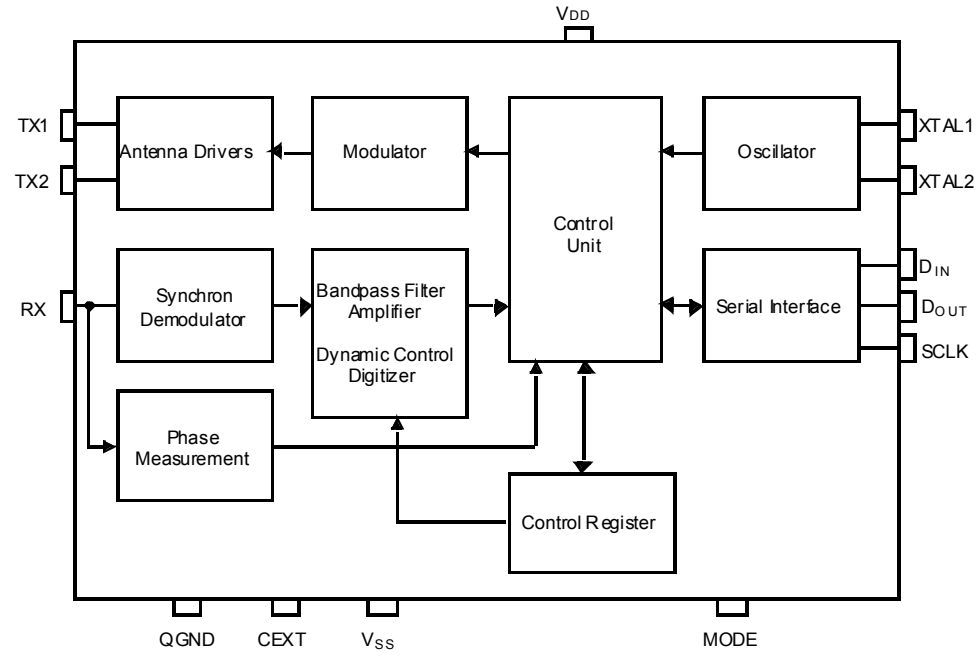


Figure 1. Blockdiagram advanced basestation PCF7991AT

5 QUICK REFERENCE DATA

PARAMETER	VALUE		
	MIN.	MAX.	UNIT
Supply voltage	4.5	5.5	V
Power-down current		20	μA
Clock/Oscillator frequency (antenna carrier frequency 125 kHz)	4	16	MHz
Antenna driver current		400	mA_p
Receiver sensitivity	2		mV_{pp}
Serial interface	CMOS compatible		
Package	SO14		
Operation temperature range	˜40°C to +85°C		

6 PINNING

6.1 Pinning Diagram

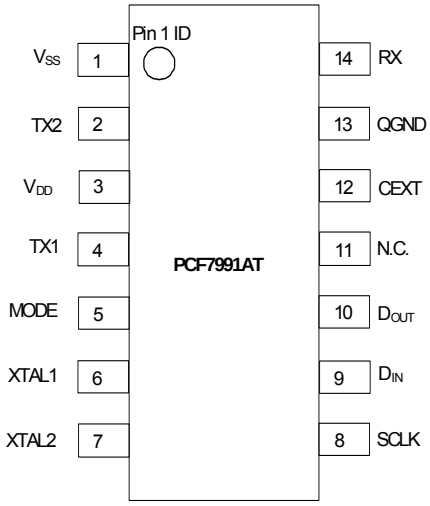


Figure 2. Pinning diagram for PCF7991AT

6.2 Pinning Information

Table 1 Pin Description for PCF7991AT

SYMBOL	PIN	DESCRIPTION
V_{SS}	1	Common ground, GND.
TX2	2	Antenna driver output.
V_{DD}	3	Supply voltage input, stabilized.
TX1	4	Antenna driver output.
MODE	5	Microcontroller interface mode select.
XTAL1	6	Oscillator interface, external clock reference input.
XTAL2	7	Oscillator interface.
SCLK	8	Microcontroller interface: serial clock input.
D_{IN}	9	Microcontroller interface: serial data in.
D_{OUT}	10	Microcontroller interface: serial data out.
N.C.	11	Not connected.
CEXT	12	High pass filter decoupling.
QGND	13	Analog ground bias.
RX	14	Receiver input.

7 MINIMUM APPLICATION CIRCUITRY

Figure 3 shows a minimal application circuitry for the PCF7991AT. The antenna coil La together with the capacitor Ca form a series resonant LC circuit (f = 125 kHz). The antenna tap voltage is attenuated by RV and the input impedance of the RX-pin. The capacitors at XTAL1 and XTAL2 are selected according to the crystal or ceramic resonator specification. In the case of an external clock reference they may be omitted. The capacitors at QGND and CEXT are for device internal biasing and decoupling purposes.

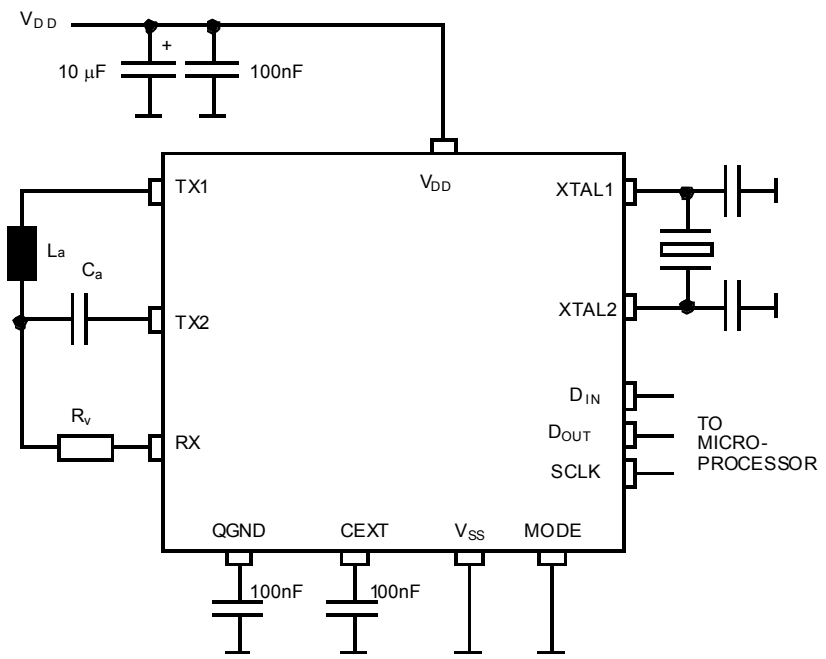


Figure 3. Minimum application circuitry

8 FUNCTIONAL DESCRIPTION

8.1 Power Supply

The PCF7991AT operates from an external 5 V power supply. For optimum performance a stabilized supply voltage should be applied.

8.2 Antenna driver

The antenna drivers are configured as a full bridge capable to deliver a square wave shaped voltage to the series resonant antenna circuit, which is connected between TX1 and TX2. The full bridge drivers are characterized by a low output impedance featuring a large drive voltage to the resonant antenna circuit. The antenna carrier frequency is 125 kHz typically.

8.3 Modulator

The modulator enables ASK (Amplitude Shift Keying) modulation of the antenna RF signal after switching the device into transparent mode (WRITE_TAG mode) by a WRITE_TAG or WRITE_TAG_N command (see Table 2). ASK modulation is achieved by blanking the antenna drive signal under control of the data input (D_{IN}). The modulator features a timer circuitry that supports carrier blanking with a programmable duration (see Table 2).

8.4 Oscillator

The on-chip oscillator operates either with a crystal or ceramic resonator connected to XTAL1/2. Alternatively, an external clock source (CMOS compatible) may be applied at XTAL1. The oscillator frequency feeds a programmable divider in order to derive the system clock and the antenna carrier frequency of 125 kHz. The programmable divider supports an oscillator frequency of 4, 8, 12 and 16 MHz (see Table 11).

8.5 Receiver

The receiver senses and demodulates the absorption modulation applied by a transponder that is inside the antenna RF field. The demodulated and digitized signal is available at the data output (D_{OUT}) after switching the device into transparent mode (READ_TAG mode) by a READ_TAG command (see Table 2).

The receiver features a high sensitivity and an extended input voltage range to ensure a large receiver dynamic range. The antenna tap signal is fed to the receiver input (RX) after attenuation by means of an external series resistor (RV) and the receiver input impedance (RIRX) in order to match the receiver input voltage specification. The receive signal passes an on-chip second order low pass filter and is further attenuated before it is fed to the synchron demodulator and phase measurement circuitry.

8.5.1 Synchron Demodulator

The antenna current and therefore the tap voltage is modulated by the transponder in amplitude and/or phase depending on various system parameters. By employing a unique Adaptive Sampling Time (AST) demodulation technique, amplitude and phase modulation of the receive signal is detected featuring an extended system operation range. The receive sampling time is set by the SET_SAMPLING_TIME command (see Table 2). The appropriate sampling time can be derived from an on-chip phase measurement and an offset that accounts for the external antenna interface component values.

Receive signal sampling is inhibited when a WRITE_TAG or WRITE_TAG_N command is issued in order to avoid that write pulses de-sensitize the amplifier and digitizer circuitry. Signal sampling is resumed when the WRITE_TAG mode is terminated. For better receiver setting a short delay after the last write pulse has to be provided before the WRITE_TAG mode is terminated.

8.5.2 Bandpass Filter, Amplifier and Digitizer

After demodulation the receive signal passes a baseband filter and amplifier prior to digitization. The amplifier gain and bandpass filter cutoff frequencies are adjustable by the SET_CONFIG_PAGE 0 command, in order to adapt the receiver path to the system coupling factor and transponder data rate.

For fast receiver settling after device power-up, sampling time shift or when switching from WRITE_TAG mode to READ_TAG mode the bandpass filter, amplifier and digitizer circuit biasing condition can be initialized and restored by a set of control bits accessible via the SET_CONFIG_PAGE commands.

8.5.3 Phase Measurement

The optimum receive signal sampling time depends on the actual tuning condition of the resonant antenna circuitry. The actual tuning condition of the resonance antenna is determined by measuring the phase relationship between the exciting signal at the antenna driver output and the antenna tap voltage applied to the receiver input. In case of perfect tuning, the phase should be 90 degree plus an offset that accounts for the receiver input attenuation and low pass filter. Miss-tuning of the resonance antenna circuit by component spreads or due to ambient temperature changes results in a change of the phase relationship. The actual phase relationship is determined by a READ_PHASE command (see Table 6) and used to

calculate the optimum receive signal sampling time with support of an external microcontroller.

8.5.4 Determing the Sampling Time

Measurement, calculation and setting of the sampling time is typically implemented during system power-up initialization when the transponder is also in its power-up sequence not sending any data. As soon as the oscillator and resonance antenna circuit are settled a phase measurement is initiated and the sampling time determined according to the following relation:

$T_S = 2 * T_{ANT} + T_{OFFSET}$

T_S	Receive signal sampling time
T_{ANT}	Actual phase measurement
T_{OFFSET}	Offset that accounts for the phase shift due to the antenna tap voltage attenuation and low pass filtering

After setting the sampling time the receiver has to settle before data can be demodulated and digitized properly.

8.5.5 Data Amplitude Comparison

For advanced receiver sampling time optimization the demodulated data signal strength can be weighted by amplitude comparison and the result reported in the status bit AMPCOMP (see Table 13).

When the ACQAMP control bit (see Table 10) is set by a SET_CONFIG_PAGE command, the actual demodulated data signal amplitude is stored as reference. After resetting the ACQAMP control bit the status bit AMPCOMP is set, when the actual data signal amplitude is larger than the stored reference otherwise it is cleared.

8.5.6 System Diagnostics

In order to detect an antenna short or open condition the receiver input voltage at the RX-pin is monitored and an antenna fail condition is reported in the status bit ANTFAIL, (see Table 13). If the receiver input voltage does not exceed the diagnostic threshold level VDTH (see Chapter 11), the status bit ANTFAIL is set, otherwise it is cleared. The status bit is updated once per antenna carrier period and can be read by a GET_CONFIG_Page 2 or 3 command (see Table 13). The status bit is undefined in Power-down or Idle mode, during the oscillator start-up time and when the antenna drivers are disabled. Advanced system diagnostics are feasible by considering the phase measurement information also.

8.6 Power-On Reset

The device generates an internal power-on reset to initialize the chip after power-on or power fail condition. As a result the control register is initialized according to Table 11.

8.7 Power-Down Modes

After a power-on reset condition the device operates in ACTIVE mode. The PCF7991AT supports an Idle and Power-down mode for power saving means. The mode of operation is determined by control bits addressed by an SET_CONFIG_PAGE 1 command (see Table 10).

In Idle mode only the oscillator and a minimum of other circuitry is active. In Power-down mode the device is in OFF state completely. The serial interface is operational in any case in order to provide access to the control register.

8.8 Serial Interface

The communication between the PCF7991AT and the microcontroller is done via a three wire digital interface. The interface is used to issue commands for writing and reading of device configuration data and for writing to and reading from the transponder in one of the transparent modes (READ_TAG, WRITE_TAG / WRITE_TAG_N). Device configuration is stored in a control register with read back feature.

The interface is operated by the following signals:

SCLK	Clock
D_{IN}	Data Input
D_{OUT}	Data Output

SCLK and D_{IN} are realized as Schmitt-Trigger inputs. D_{OUT} is an open drain output with a weak internal pull-up resistor.

Any communication between the PCF7991AT and the microcontroller begins with an initialization of the serial interface before the desired command can be issued. The interface initialization condition is a low-to-high transition of the signal D_{IN} while SCLK is high (see Figure 4).

All commands are transmitted to the PCF7991AT serial interface starting with Most Significant Bit (MSB). D_{IN} is latched with a high state at SCLK. D_{OUT} is valid during the high state of SCLK (MODE pin connected to VSS).

D_{OUT} and D_{IN} may be connected to each other in order to form a two-wire communication link with the microcontroller (always half duplex communication).

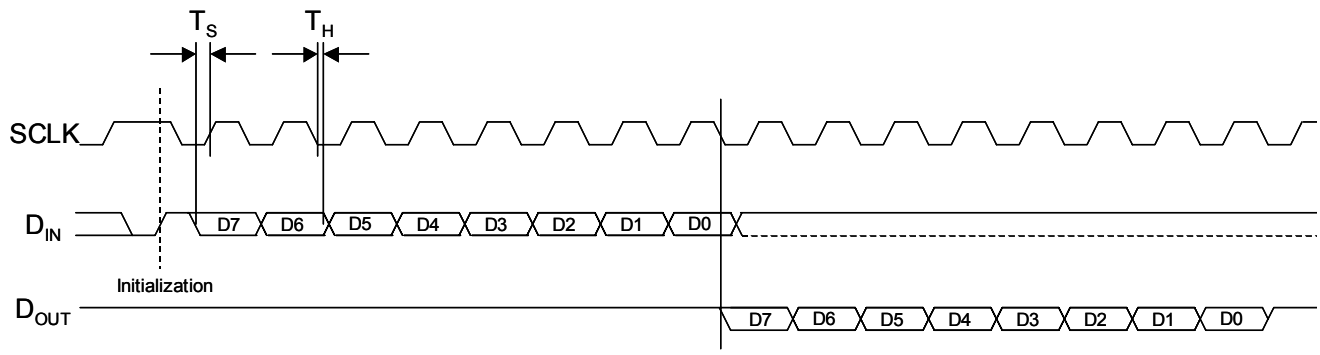


Figure 4. Serial Interface Timing

8.8.1 Serial Interface Mode

The serial interfaces supports two modes of operation, filtered and non-filtered communication.

If MODE is connected to VSS, no filtering is applied and the state of the interface signals is directly available at the internal circuitry. The maximum data rate of the serial interface is limited by the set-up and hold time as specified (see Chapter 11.2).

If MODE is connected to VDD, digital filtering of SCLK and D_{IN} is performed offering improved immunity against glitches, reflections and EMC on these interface signals. This mode of operation is intended for use for so-called 'Active Antenna Applications', where the PCF7991AT and the microcontroller have to communicate via long interface wires.

The digital filtering is provided by sampling the SCLK and D_{IN} inputs at a rate of $1/f_{TX}$, 8 µs typically. The internal state of these signals is updated only after two successive samples of the same logic level. The result of this evaluation is delayed by another 8µs. Hence, all state changes at the SCLK or D_{IN} inputs are delayed by 16µs to 24 µs, until they are recognized by the internal circuitry.

When filtered SPI communication is used, it must be avoided that a level change of both input signals occurs in the same sampling period. The setup time becomes (Figure 5):

$$T_{S,MODE1} = 1/f_{TX} + T_{S,MODE0} + T_H$$

The absolute accuracy of f_{TX} has to be considered for the calculation of the minimum value of $T_{S,MODE1}$.

If D_{IN} and D_{OUT} are connected to each other to form a two-wire communication link, the filtering delay between D_{IN} and D_{OUT} must be considered in order to meet $T_{S,MODE1}$. Since data at pin D_{OUT} is clocked out with the negative edge of the deglitched signal SCLK, the maximum propagation delay between the negative edge of SCLK and the change of D_{OUT} has to be considered (Figure 6):

$$T_{DOUT,MODE1,max} = 3/f_{TX,min} + T_{S,MODE0} + T_{DEL}$$

The additional delay T_{DEL} depends on the external circuitry (e.g. caused by line drivers or capacitive loads) and is calculated to be:

$$T_{DEL} \cong 5 * (C_{DOUT} + C_{EXT}) (R_P \parallel R_{EXT})$$

In Figure 7, the maximum delays to be considered for two-wire communication are summarized in a block diagram.

If digital filtering of SCLK and D_{IN} is enabled and the device has been forced into Power-down mode, this mode can be terminated by setting SCLK to LOW and D_{IN} unequal to the status bit TXDIS (see Table 10). As a result, the XTAL oscillator is restarted and the configuration bit PD_MODE is cleared, which causes the device to enter Idle mode.

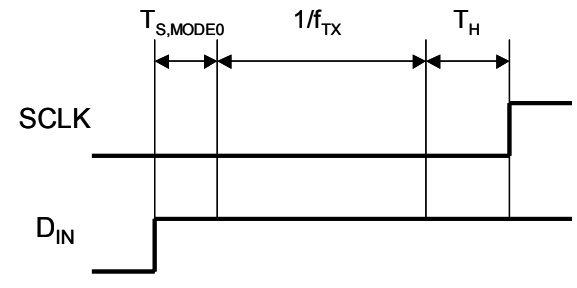


Figure 5. Setup time for D_{IN} and SCLK for filtered SPI communication

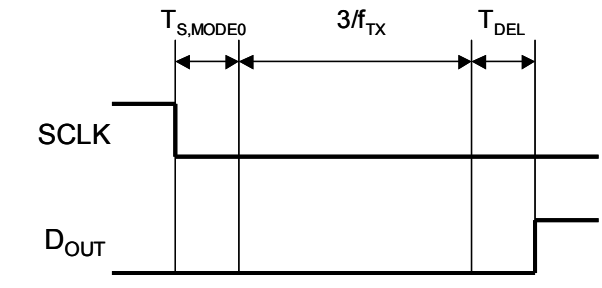


Figure 6. Max. output delay for DOUT for filtered SPI communication (two-wire communication)

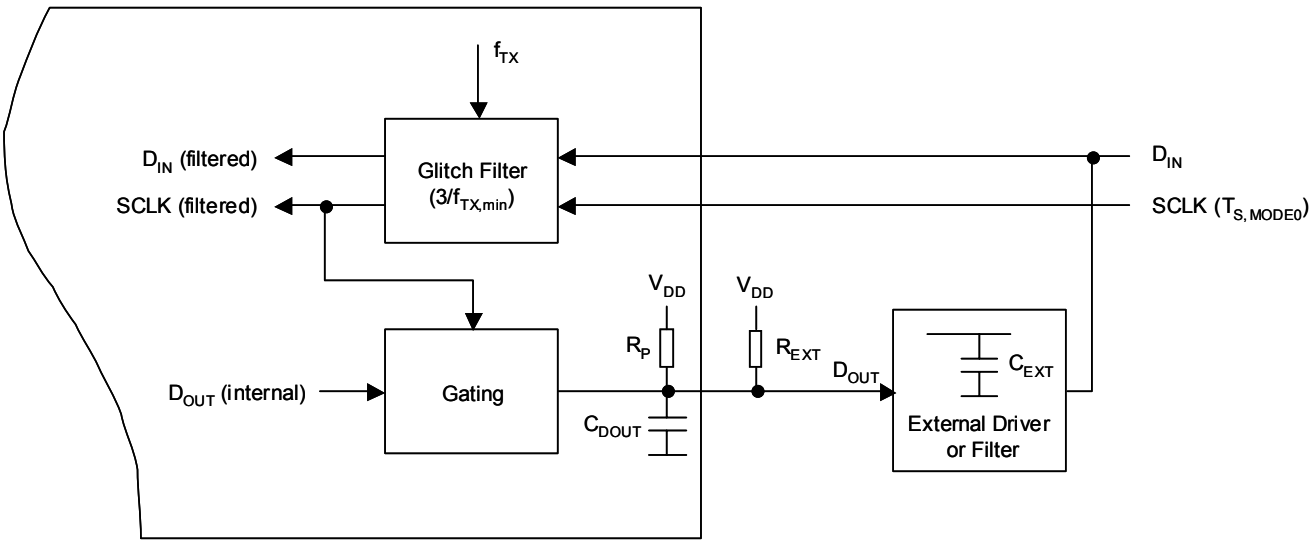


Figure 7. Filtering delay during two-wire communication

9 COMMAND SET

Table 2 Command set summary

COMMAND NAME	MSB BIT NO. LSB								RESPONSE
	7	6	5	4	3	2	1	0	
GET_SAMPLING_TIME	0	0	0	0	0	0	1	0	8 bit (0 0 D5-D0)
GET_CONFIG_PAGE	0	0	0	0	0	1	P1	P0	8 bit (X3 X2 X1 X0 D3-D0)
READ_PHASE	0	0	0	0	1	0	0	0	8 bit (0 0 D5 - D0)
READ_TAG	1	1	1	-	-	-	-	-	enter READ_TAG-mode
WRITE_TAG_N	0	0		1	N3	N2	N1	N0	enter WRITE_TAG-mode with pulse width programming
WRITE_TAG	1	1	0	-	-	-	-	-	enter WRITE_TAG-mode
SET_CONFIG_PAGE	0	1	P1	P0	D3	D2	D1	D0	4 bit per config page addressed
SET_SAMPLING_TIME	1	0	D5	D4	D3	D2	D1	D0	8 bit (00 D5 - D0)

9.1 READ_TAG

This command is used to read the demodulated bit stream from a transponder: After the assertion of the three command bits the PCF7991AT instantaneously switches to READ_TAG-mode and the demodulated, filtered and digitized data from the transponder is available at the data output D_{OUT} for decoding by the microcontroller.

READ_TAG-mode is terminated immediately by a low to high transition at SCLK.

Table 3 READ_TAG command sequence

BIT NO.	7	6	5	4	3	2	1	0	REMARK
Command	1	1	1	-	-	-	-	-	received data available at D_{OUT}

9.2 WRITE_TAG_N

This command is used to write data to a transponder and to set the modulator blanking characteristics.

If N3-N0 are set to zero, the signal from D_{IN} is transparently switched to the drivers. A high level at D_{IN} corresponds to antenna drivers switched off, a low level corresponds to antenna drivers switched on.

If any binary number between 1 and 1111 is loaded into N3-N0, the drivers are switched off at the next positive transition of D_{IN}. The driver off state is maintained for a time interval equal to N * T0 (T0=8 μs) regardless the state of D_{IN}. This method relaxes the timing resolution requirements to the microcontroller and to the software implementation while providing an exact, selectable write pulse timing.

WRITE_TAG-mode is terminated immediately by a low to high transition at SCLK. As a result, the driver resume their initial state, regardless the actual state of the modulation pulse timer.

Table 4 WRITE_TAG_N command sequence

BIT NO.	7	6	5	4	3	2	1	0	REMARK
Command	0	0	0	1	N3	N2	N1	N0	no response

9.3 WRITE_TAG

This is the 3 bit short form of the command WRITE_TAG_N. It allows to switch into WRITE_TAG-mode with a minimum communication time.

The behaviour of the WRITE_TAG command is identical to WRITE_TAG_N with two exceptions:

WRITE_TAG-mode is entered after assertion of the 3rd command bit.

No N parameter is specified with this command; instead the N value which has been programmed with the most recent WRITE_TAG_N command is used. If no WRITE_TAG_N was issued so far, a default N=0 (transparent mode) will be assumed.

WRITE_TAG-mode is terminated immediately by a low to high transition at SCLK. As a result, the driver resume their initial state, regardless the actual state of the modulation pulse timer.

Table 5 WRITE_TAG command sequence

BIT NO.	7	6	5	4	3	2	1	0	REMARK
Command	1	1	0	-	-	-	-	-	no response

9.4 READ_PHASE

This command is used to read the antenna´s phase T_{ANT}, which is measured at every carrier cycle. The phase is coded binary in D5-D0.

Table 6 READ_PHASE command sequence

BIT NO.	7	6	5	4	3	2	1	0	REMARK
Command	0	0	0	0	1	0	0	0	
Response	0	0	D5	D4	D3	D2	D1	D0	

9.5 SET_SAMPLING_TIME

This command specifies the demodulator sampling time Ts. The sampling time is coded binary in D5-D0.

Table 7 SET_SAMPLING_TIME command sequence

BIT NO.	7	6	5	4	3	2	1	0	REMARK
Command	1	0	D5	D4	D3	D2	D1	D0	no response

9.6 GET_SAMPLING_TIME

This command is used to read back the sampling time Ts set with SET_SAMPLING_TIME. The sampling time is coded binary in D5-D0.

Table 8 GET_SAMPLING_TIME command sequence

BIT NO.	7	6	5	4	3	2	1	0	REMARK
Command	0	0	0	0	0	0	1	0	
Response	0	0	D5	D4	D3	D2	D1	D0	

9.7 SET_CONFIG_PAGE

This command is used to configure the receiver characteristics (cutoff frequencies, gain factors) and the different operation modes. P1 and P0 select one of four configuration pages.

Table 9 SET_CONFIG_PAGE command sequence

BIT NO.	7	6	5	4	3	2	1	0	REMARK
Command	0	1	P1	P0	D3	D2	D1	D0	no response

Table 10 SET_CONFIG_PAGE mapping

BIT NO. COMMAND/PAGE NO.	P1	P0	D3	D2	D1	D0
SET_CONFIG_PAGE 0	0	0	GAIN1	GAIN0	FILTERH	FILTERL
SET_CONFIG_PAGE 1	0	1	PD_MODE	PD	HYSTERESIS	TXDIS
SET_CONFIG_PAGE 2	1	0	THRESET	ACQAMP	FREEZE1	FREEZE0
SET_CONFIG_PAGE 3	1	1	DISLP1	DISSMART COMP	FSEL1	FSEL0

Table 11 Configuration bit description

BIT NAME	DESCRIPTION	RESET CONDITION	
FILTERL	main low pass cutoff frequency	0	0: f_L = 3 kHz; 1: f_L = 6 kHz
FILTERH	main high pass cutoff frequency	0	0: f_H = 40 Hz; 1: f_H = 160 Hz
GAIN0	amplifier_0 gain factor	0	0: $gain_0$ = 16; 1: $gain_0$ = 32
GAIN1	amplifier_1 gain factor	1	0: $gain_1$ = 6.22; 1: $gain_1$ = 31.5
TXDIS	disable antenna driver	0	0: driver active; 1: driver inactive
HYSTERESIS	data comparator hysteresis	0	0: hysteresis OFF; 1: hysteresis ON
PD	Power-down mode enable	0	0: device active; 1: Power-down mode
PD_MODE	select Power-down mode, if PD = 1	0	0: Idle mode; 1: Power-down mode
FREEZE0	receiver characteristics override	0	Note 1
FREEZE1	receiver characteristics override	0	Note 1
ACQAMP	store signal amplitude as reference for later amplitude comparison	0	see Section 8.5.5
THRESET	reset threshold generation of digitizer	0	Note 3
FSEL0	clock frequency select LSB	0	Note 2
FSEL1	clock frequency select MSB	0	
DISSMARTCOMP	disable smart comparator	0	0: comparator = ON, 1: comparator = OFF
DISLP1	disable main low pass	0	0: low pass = ON, 1: low pass = OFF

Note

1. In order to achieve fast receiver settling the amplifier and filter characteristics can temporarily be overridden:

FREEZE 1	FREEZE 0	REMARK
0	0	normal operation according to configuration page 0
0	1	main low pass is frozen and main high pass is initialized to QGND
1	0	main low pass is frozen and the time constant of the main high pass is reduced by a factor of 16 for FILTERH = 0 and by a factor of 8 for FILTERH = 1
1	1	time constant of the main high pass is reduced by a factor of 16 for FILTERH = 0 and by a factor of 8 for FILTERH = 1. Second high pass is initialized to QGND

2. In order to derive an antenna carrier frequency f_{TX} of 125 kHz; the clock divider has to be programmed as follows:

FSEL1	FSEL0	OSCILLATOR FREQUENCY
0	0	4 MHz
0	1	8 MHz
1	0	12 MHz
1	1	16 MHz

3. If the THRESET is set, the threshold generator is disabled and initialized according to the receive signal conditions.

9.8 GET_CONFIG_PAGE

This command has three functions:

1. Reading back the configuration parameters set by SET_CONFIG_PAGE command
2. Reading back the transmit pulse width programmed with WRITE_TAG_N
3. Reading the system status information

P1 and P0 select one of four configuration pages. The response (X3 X2 X1 X0 D3 D2 D1 D0) contains the contents of the selected configuration page in its lower nibble. For P = 0 or P = 1 the higher nibble reflects the current setting of N (the transmit pulse width). For P = 2 or P = 3 the system status information is returned in the higher nibble.

Table 12 GET_CONFIG_PAGE command sequence

BIT NO.	7	6	5	4	3	2	1	0	REMARK
Command	0	0	0	0	0	1	P1	P0	
Response	X3	X2	X1	X0	D3	D2	D1	D0	

Table 13 GET_CONFIG_PAGE mapping

COMMAND / PAGE NO.	BIT NUMBER							
	7	6	5	4	3	2	2	0
GET_CONFIG_PAGE 0	N3	N2	N1	N0	D3	D2	D1	D0
GET_CONFIG_PAGE 1	N3	N2	N1	N0	D3	D2	D1	D0
GET_CONFIG_PAGE 2	0	0	AMPCOMP	ANTFAIL	D3	D2	D1	D0
GET_CONFIG_PAGE 3	0	0	AMPCOMP	ANTFAIL	D3	D2	D1	D0

Table 14 Status Bit description

BIT NAME	DESCRIPTION	
ANTFAIL	antenna failure	see Section 8.5.6
AMPCOMP	amplitude comparison result	see Section 8.5.5

10 LIMITING VALUES

All values are in accordance with Absolute Maximum Rating System (IEC 134)

PARAMETER	MIN.	MAX.	UNIT
Operating temperature range	-40	+85	°C
Storage temperature range	-65	+125	°C
Junction temperature		+140	°C
Voltage at any pin to ground, except pin RX	-0.3	+6.5	V
Voltage at any pin to ground, except pins RX, D_{IN}, D_{OUT}, SCLK	-0.3	V_{DD} +0.3	V
Voltage at pin RX to ground	-10	+12	V
Input current for pins D_{IN}, D_{OUT}, SCLK		10	mA
ESD, human body model, Note 1		2	kV
Power dissipation		200	mW

Note

1. According to MIL-STD 883D, Method 3015, 7d

11 ELECTRICAL CHARACTERISTICS

11.1 DC Characteristics

T_{amb} = -40 to +85°C, V_{DD} = 5.5V, V_{SS} = 0V, unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	Supply voltage	With respect to V_{SS}	4.5	5.0	5.5	V
I_{ON}	Operating supply current	$I_{TX1} = I_{TX2} = 0$		4.0	10	mA
I_{ID}	Supply current, IDLE mode	Note 1		0.2	0.4	mA
I_{PD}	Supply current, Power-Down mode	Note 1		7.0	20	μA
Antenna Driver (TX1, TX2)						
I_{TXCW}	Output peak-current	Continuous wave			200	mA_p
$I_{TXpulse}$	Output peak-current	On/Off-ratio = 1:4 t_{on} < 400 ms			400	mA_p
R_{OTX}	Output resistance	Full bridge, $R_{OTX} = R_{OTX1} + R_{OTX2}$		2.5	7.0	Ω
Receiver input (RX)						
V_{IRX}	Input voltage range	With respect to QGND	-8		+8	V_p
V_{QGND}	Analog ground		0.35 V_{DD}	0.42 V_{DD}	0.50 V_{DD}	V
R_{IRX}	Input impedance		17	25	33	kΩ
V_{DTH}	Diagnostic threshold level	With respect to QGND	-1.5	-1.15	-0.8	V
Serial Interface (D_{IN}, D_{OUT} , SCLK)						
Data Input, serial input ($D_{IN,}$ SCLK)						
V_{IL}	Input voltage LOW		-0.3		0.3 V_{DD}	V
V_{IH}	Input voltage HIGH		0.7 V_{DD}		V_{DD} +0.3	V
I_{IL}	Input current LOW	V_{IH} = 0V			-2	μA
I_{IH}	Input current HIGH	$V_{IH} = V_{DD}$			+2	μA
Digital output (D_{OUT})						
V_{OL}	Output voltage LOW	I_{OL} < 1 mA			0.4	V
I_{OL}	Output current LOW	$V_{OL} \leq 0.4$ V	1			mA
I_{OPU}	Output current HIGH	V_{OL} = 0 V	-10			μA

Note

1. Does not include power consumption of XTAL or other external components.

11.2 AC Characteristics

T_{amb} = -40 to +85°C, V_{DD} = 5.5V, V_{SS} = 0V, f_{TX} = 125 kHz; unless otherwise specified

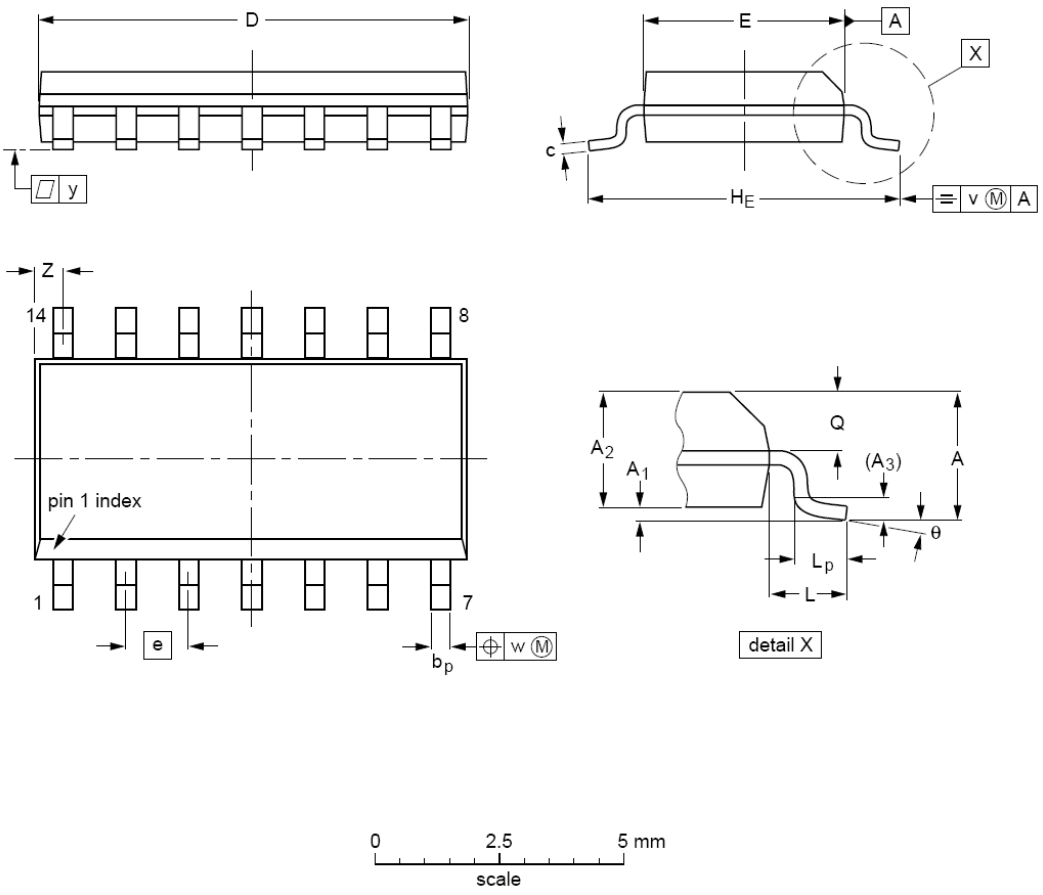
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
XTAL Oscillator (XTAL1, XTAL2)						
f_{OSC}	Frequency range	Depending on FSEL	4		16	MHz
T_{SUP}	Start-up time			4	10	ms
R_{FB}	Feedback resistance	XTAL1 to XTAL 2	0.5	1.3	3	MΩ
External Clock Input (XTAL1)						
f_{EXT}	Frequency range	Depending on FSEL	4		16	MHz
	Duty cycle		40		60	%
C_{XTAL1}	Input capacitance	XTAL1		5		pF
Serial Interface						
$T_{S,MODE0}$	Set-up time	MODE pin at V_{SS}	50			ns
T_H	Hold time	MODE pin at V_{SS}	50			ns
C_{DOUT}	Output Capacitance	MODE pin at V_{SS}			15	pF
C_{IN}	Input Capacitance			3	7	pF
Receiver						
V_{RX}	Receiver sensitivity	With respect to QGND	2	1		mV_{pp}
T_{RCV0}	Receiver delay	FILTER = 0	290	310	340	μs
T_{RCV1}	Receiver delay	FILTER = 1	160	175	190	μs
	Phase measurement error				± 5.7	°
Recovery from clock stable to demodulator valid						
T_{RPD}	Recovery time demodulator	Note 1			5	ms
Recovery from WRITE-pulse						
T_{RWD}	Recovery time demodulator	Note 1			500	μs
Recovery from AST-step						
T_{RAST}	Recovery time demodulator	Note 1		0.7	1.5	ms
Response delay data input to antenna driver						
TDITX	Response delay DIN to TX	MODE pin at VSS; Note 2			10	□s

Note

1. Specific command sequence required.
2. Applicable for WRITE_TAG and WRITE_TAG_N commands. Due to device internal signal synchronization measures, T_{DITX} is the response delay between a change at D_{IN} and the resulting change at the antenna drivers. In the case of N is zero, T_{DITX} applies for both the rising and failing transition at D_{IN}, while for N unequal zero it applies for the rising transition at D_{IN} only.

12 PACKAGE OUTLINE

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT108-1	076E06S	MS-012AB				~~95-01-23~~ 97-05-22

13 REVISION HISTORY

Revision	Page	Description
2007 Aug 15		Change to NXP style
		Editorial updates and corrections
	3	Statement for compatibility to HT2-Extended and HT-Pro Family added
	8-9	Chapter 8.8 “Serial Interface Description” extended
	10	Figures 5 to 7 added
	16-18	LIMITING VALUES, DC CHARACTERISTICS and AC CHARACTERISTICS adopted according to Product Specification Annex, 2000 Sep 18
	18	Specification of Output Capacitance C_{DOUT} added

14 LEGAL INFORMATION

14.1 Data sheet status

Document status	Product status	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification or product development
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification
Product [short] data sheet	Production	This document contains the product specification

14.2 Definitions

Draft

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